

IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 29. This sheet, which includes Fig. 29, replaces the original sheet including Fig. 29.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-22 are presently pending in this case, Claims 1-3, 5, 8, and 11-12 having been amended, Claims 9-10 having been canceled, and Claims 21-22 having been added by the present amendment, and Claims 3 and 13-20 having been withdrawn from consideration and Drawing corrections having been made to designate Fig. 29 as --Prior Art--.

In the outstanding Official Action, Claims 3 and 13-20 were withdrawn as being drawn to a non-elected invention; the drawings were objected to under 37 CFR §1.83(a) as not showing the subject matter of Claim 8; Claim 2 was objected to because of informalities; Claims 8-12 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; Claims 1 and 4-6 were rejected under 35 U.S.C. 102(e) as being anticipated by Herbert, U.S. Patent 6,888,207 (the '207 reference); Claim 2 was rejected under 35 U.S.C. 102(b) as being anticipated by Kumagai, U.S. Patent 6,057,568 (the '568 reference); Claims 1-2 and 4-7 were rejected under 35 U.S.C. 102(b) as being anticipated by Shimomura et al, U.S. Patent 6,140,687 (the '687 reference).

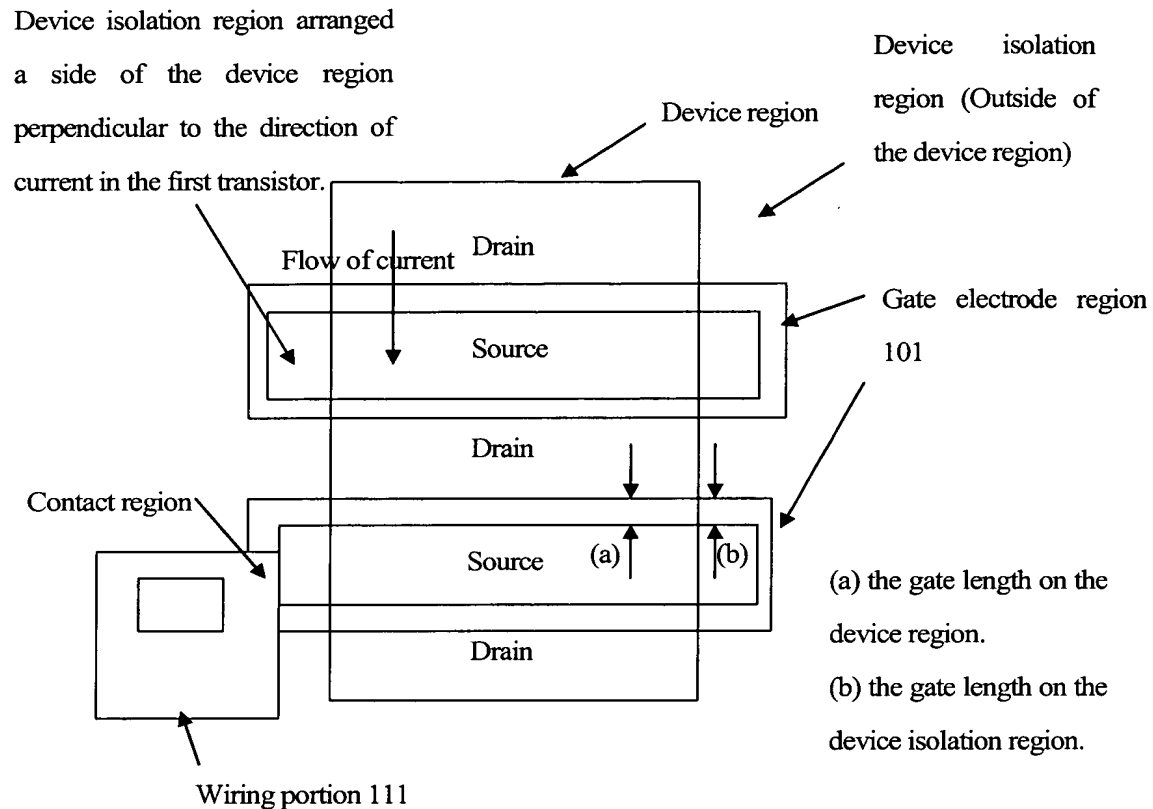
First, with respect to the withdrawal of Claim 3 as directed to a non-elected invention, Applicants respectfully request reconsideration of this withdrawal, because upon further review and consideration, Applicants believe that Claim 3 in fact falls within the elected Species I as Claim 3 recites an inverter shown in Fig. 1. Reconsideration of the withdrawal of Claim 3 and examination on the merits of Claim 3 are therefore respectfully requested.

In response to the objection to Figure 29, submitted herewith is a replacement sheet for Fig. 29 wherein Fig. 29 is designated by the legend --Prior Art--. Accordingly, the objection to Fig. 29 is believed to have been overcome.

Applicants respectfully traverse the objection to the drawings as not showing the subject matter of Claim 8. Claim 8 recites,

8. The semiconductor device of claim 1, wherein respective loop-shaped gate electrode regions have same lengths on the device region and a device isolation region except contact regions between wiring portions and the gate electrode regions.

Thus, in Claim 8, the loop-shaped gate electrode region has same length on the device region and the device isolation region. As shown in Reference Figure 1 presented on the next page of this paper, (a) is the gate length on the device region and (b) is the gate length on the device isolation region. The “exception” in Claim 8 regarding the contact regions between the wiring portions and the gate electrode regions arises because the length of the contact portion connected to the wire portion of the loop-shaped gate electrode is sometimes lengthened for secure connection to the wire portion, as shown in the left bottom portion of the Reference Figure 1. This structure further distinguishes over the Kumagai reference, which in Fig. 4A shows a gate 108a which has shorter channel region (right side) than others. Nevertheless, it is respectfully submitted that the subject matter of Claim 8 is shown in Figure 1 of the present application, and withdrawal of the objection to Claim 8 is respectfully requested.



**REFERENCE FIG. 1**

The outstanding rejection of Claim 8 under 35 USC §112, 2<sup>nd</sup> para., was based on the finding that the recitation that “the respective loop-shaped gate electrode regions have same lengths on the device region and a device isolation region except contact regions between wiring portions and the gate electrode regions” in the Claim 8 does not have a proper antecedent basis and that it is not clear what sections of the loop-shaped gate electrode region

have the same length and/or with respect to what exception. In response, Claim 8 has been amended to delete reference to “the” in referring to “respective loop shaped gate electrode regions.” Further, as explained above in regard to the above Reference Figure 1, in this figure, (a) is the gate length on the device region and (b) is the gate length on the device isolation region, as is believed apparent to persons skilled in the art from Figure 1 of Applicants’ disclosure. Accordingly, the rejection of Claim 8 under of 35 USC §112, 2<sup>nd</sup> para., is believed to have been overcome. If the Examiner disagrees, the Examiner is requested to clarify the basis of the rejection and/or make suggestions as to how this ground for rejection can be overcome.

Turning now to the rejection of Claim 1 under 35 USC 102 (e) as being anticipated by Herbert, Herbert discloses high voltage MOSFETs with graded extensions that provide a high breakdown voltage. In Fig. 3, Herbert discloses a ring-gate geometry 300 forming a ring with gate polysilicon 355 and gate oxide 354 to create a ring-gate electrode which surrounds N+ drain region 363, N-drift 356, N-well 360, and HV P-well 359. Ring-gate geometry 300 eliminates any risk of premature drain edge breakdown, also known as termination breakdown, from drain region 363 to the isolation region created by gate electrode ring 355. The ring-gate geometry 300 encloses the drain area in Fig. 3 (and Claim 2). The word “enclose” means to surround and confine within a limited area (The American Heritage® Dictionary of the English Language, Fourth Edition copyright ©2000). In contrast, the loop-shaped electrode region of claimed semiconductor is arranged to surround a part of the device region and a device isolation region. This feature is shown, for instance, in Figs. 1 and 2. Claim 5 has been amended to clarify that a plurality of electrically independent drain regions are formed in a region surrounded by the loop-shaped electrode region. This feature is shown in Fig. 3 (102a and 102b).

With respect to the outstanding rejection of Claim 2 under 35 USC 102(b) as being anticipated by Kumagai, Kumagai discloses a semiconductor device including P<sup>+</sup> type diffusion layers 106a, 106b, and 106c, and a P-channel MOS gate 108a and 108b. Each of P-channel MOS gate 108a, and 108b functions as a single gate electrode. The right side of the P-channel MOS gate 108a functions as a gate electrode. In contrast, each loop-shaped gate electrode of Claim 2 is disposed onto two positions between the source regions and the drain regions, and the loop-shaped electrode region is arranged to surround a part of the device region and a device isolation region. Furthermore, the loop-shaped gate electrode regions of Claim 8 have same lengths on the device region and a device isolation region except contact regions between wiring portions and the gate electrode regions. The gate electrode of Kumagai has a different length between left side and right side, which functions as a gate. In other word, the gate electrode of Kumagai functions as a single gate, and is not shared by two transistors. Accordingly, it is respectfully submitted that the rejection of Claim 12 as anticipated by Kumagai is traversed.

With regard to the rejection of Claims 1, 2 and 4 to 7 under 35 USC 102(b) as being anticipated by Shimomura et al., Shimomura et al. disclose a high frequency ring gate MOSFET including a ring gate electrode formed on a semiconductor substrate, a drain region 2 formed in the semiconductor substrate at an inside of the gate electrode 1, and a source region 3 formed in the semiconductor substrate at an outside of the gate electrode 1 and larger than the drain region 2. In contrast, each of the loop-shaped gate electrodes of the claimed device is disposed onto two positions between the source regions and the drain regions, and the loop-shaped electrode region is arranged to surround a part of the device region and a device isolation region. Furthermore, the ring gate of Shimomura et al. functions as a single gate, and is not shared by two transistors. In contrast, the claimed gate electrode is shared by

two transistors. Also, in Shimomura et al., there are wires between the ring gate region and contacts 6. This causes an increase of parasitic capacitance by which the operation speed becomes slower. The claimed gate electrode does not need wires because the electrode is arranged to surround not only a part of the device region but also a device isolation region.

Further, the structure taught by Shimomura et al. results in a different operational characteristic. In particular, in Fig. 1 of Shimomura et al., an area at the inside of the gate electrode 1 corresponds to a drain region 2, and an area at the outside of the gate electrode 1 corresponds to a source region 3 and substrate contact portions 5. Current flows from the drain region 2 to the source region 3. Since the drain region 2 is surrounded by the source region 3, the current flows in all directions. In this structure, a current may flow well in one direction, but may not flow well in a different direction. That is to say, compared with same gate width size of the straight gate shape, the average current flow rate of “surrounding type gate” is lower than that of straight gate shape transistor. In contrast, current flows in the device of the claimed invention from drain to source, that is the current flows only one way as is depicted in Reference Figure 1. To clarify the difference, Claim 21 has been added and recites that the device isolation region is arranged aside the device region perpendicular to a direction of current flowing from the first source region to the first drain region in the first transistor.

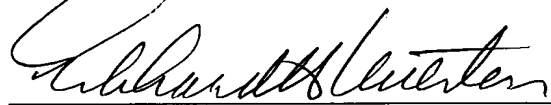
In view of the noted differences, it is respectfully submitted that the amended claims patentably define over Shimomura et al.

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Reply to Office Action of November 10, 2005

Consequently, in view of the present amendment and in light of the above comments, no further issues are believed to be outstanding, and the present application is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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